SMH Technologies®

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Driver v. 5.01

Moreno Ortolan

Interfacing FlashRunner 2.0 with ABOV MC9X

SMH Technologies S.r.l.

UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

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ABOV MC9X Introduction

ABOV's Semiconductor provides solutions such as main-stream & Display, Motor Control, Touch, Bluetooth, etc. to white goods, kitchen appliances, and smart household appliances.

Also, we design MCUs optimized for smart home appliances with energy-efficient design and provide a variety of portfolios to customers.

ABOV Semiconductor presents a wide range of 8-bit MCUs that are based on M8051 cores. We have experienced a variety of consumer electronics with them, and based on this, we can provide excellent noise immunity, code optimization, and cost savings for customer's board design.

Our 8-bit MCUs can be used for many different applications such as smart home appliance, smoke Detector, touch, and remote controller, as well as achieve smart Integration by utilizing multiple communications and rich advanced analog IPs.
Easy-to-use Ecosystem and a lot of experience of mass production are also our strength.

MC Series:

The MC series is an ABOV's CMOS 8-bit microcontroller.

The MC series has high reliability and rich history of mass production, and provides a flash memory ranging in size from 2KB to 128KB.

It is highly flexible for using various embedded control applications and supports low power mode to reduce power consumption. As a cost-effective solution, it is actively used in the white home appliances, smart home appliances, and consumer markets.

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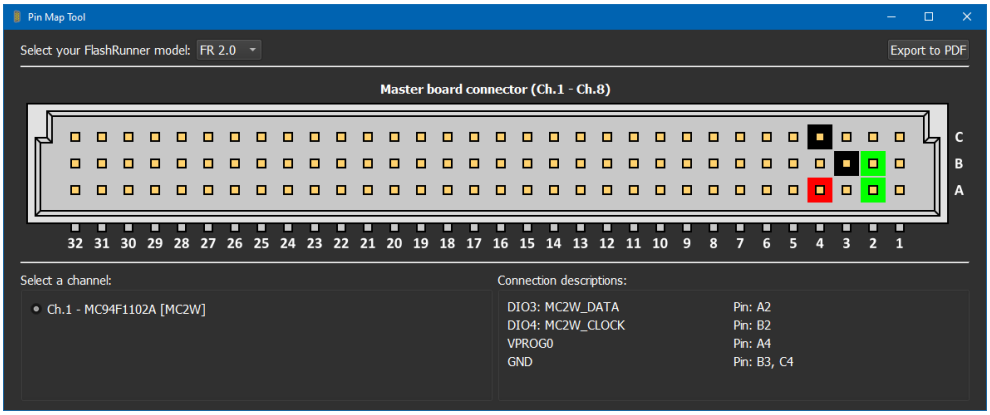
ABOV MC9X Protocol and PIN map

ABOV MC9X devices support the MC2W protocol.

```
#TCSETPAR CMODE <MC2W>
```

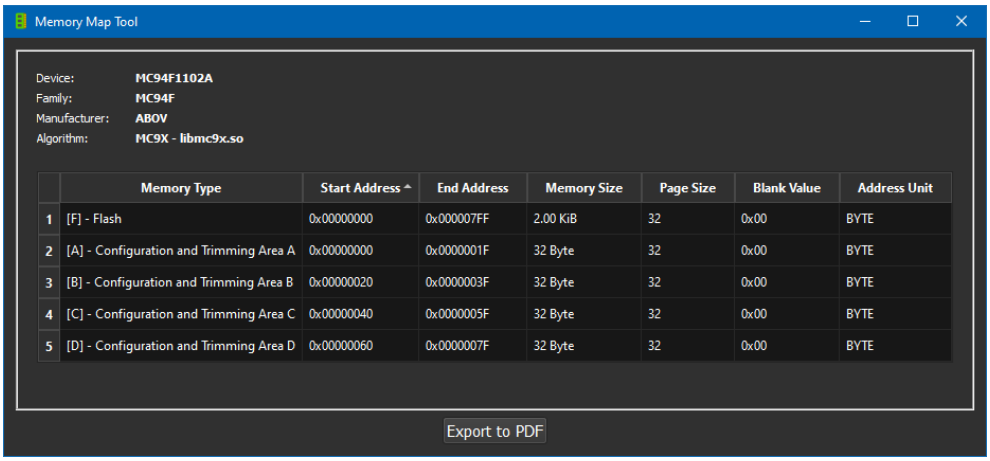
ABOV MC9X PIN MAP



ABOV MC9X Memory Map

ABOV MC94F1102A Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - Flash	0x00000000	0x000007FF	2.00 KiB	32	0x00	BYTE
[A] - Configuration and Trimming Area A	0x00000000	0x0000001F	32 Byte	32	0x00	BYTE
[B] - Configuration and Trimming Area B	0x00000020	0x0000003F	32 Byte	32	0x00	BYTE
[C] - Configuration and Trimming Area C	0x00000040	0x0000005F	32 Byte	32	0x00	BYTE
[D] - Configuration and Trimming Area D	0x00000060	0x0000007F	32 Byte	32	0x00	BYTE



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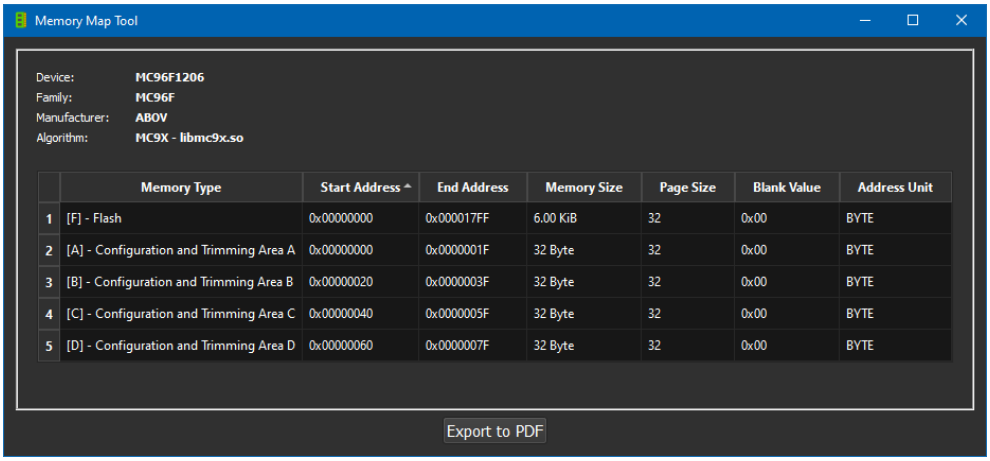
ABOV MC96F1206 Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - Flash	0x00000000	0x000017FF	6.00 KiB	32	0x00	BYTE
[A] - Configuration and Trimming Area A	0x00000000	0x0000001F	32 Byte	32	0x00	BYTE
[B] - Configuration and Trimming Area B	0x00000020	0x0000003F	32 Byte	32	0x00	BYTE
[C] - Configuration and Trimming Area C	0x00000040	0x0000005F	32 Byte	32	0x00	BYTE
[D] - Configuration and Trimming Area D	0x00000060	0x0000007F	32 Byte	32	0x00	BYTE



	Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
1	[F] - Flash	0x00000000	0x000017FF	6.00 KiB	32	0x00	BYTE
2	[A] - Configuration and Trimming Area A	0x00000000	0x0000001F	32 Byte	32	0x00	BYTE
3	[B] - Configuration and Trimming Area B	0x00000020	0x0000003F	32 Byte	32	0x00	BYTE
4	[C] - Configuration and Trimming Area C	0x00000040	0x0000005F	32 Byte	32	0x00	BYTE
5	[D] - Configuration and Trimming Area D	0x00000060	0x0000007F	32 Byte	32	0x00	BYTE

ABOV MC9X Trimming Area

Trimming and Configurations areas are subdivided in four regions named OTP A, OTP B, OTP C, OTP D.
OTP_A area is user configuration area.
Other trimming data areas are not for user (OTP_B, OTP_C, OTP_D). It contains calibration data for each device, do not erase or write this data.

MC94x Trimming Area

MC94x OTP Overview

OTP Area Information

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	...	0x1F
OTP D	IRC_TCAL										
OTP C	TRIMC0	TRIMC1	TRIMC2	TRIMC3	PT1ID	PT2ID	PT3ID	FTID	RTID		
OTP B	TRIMB0	-	-	-	-	-	-	-	-	-	-
OTP A	CFGA0	-	-	-	-	-	-	-	-	-	-

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Trimming & Configuration Area register map

Register Name	SFR ADDR	OTP Area	OTP ADDR	Register bit [7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CFG0	F8h	OTP A	00h	RSTEN	-	-	-	BSIZE[1:0]		LOCKB	LOCKF
TRIMB0	F9h	OTP B	20h	IRCCAL [7:0]							
TRIMC0	FAh	OTP C	40h	LVDSEL[1:0]		BLVD	BSSEL	HVVDD	LVDCAL[1:0]		OCDDB
TRIMC1	FBh	OTP C	41h	VDD CAL[2:0]			IRC TCAL[2:0]			WDTFCAL[1:0]	
TRIMC2	FCh	OTP C	42h	BMCAL[3:0]				TRIM[3:0]			
TRIMC3	FDh	OTP C	43h	-	-	-	-	-	-	-	-

CFG00 : Configuration area address 0x00

RSTEN	Select RESETB pin	0	Disable RESETB pin (default)
		1	Enable RESETB pin
BSIZE[1:0]	Hard Lock Size Select bit Note) When LOCKB is set, This is applied.	00	2KB – 32B (000h ~ 7DFh)
		01	2KB – 64B (000h ~ 7BFh)
		10	2KB – 128B (000h ~ 77Fh)
		11	2KB – 256B (000h ~ 6FFh)
LOCKB	Select Specific Area for Write Protection Bit	0	Hard LOCK Disable
		1	Hard LOCK Enable
LOCKF	Code Read Protection Bit	0	LOCK Disable
		1	LOCK Enable

MC94x OTP Configuration Area A

The User bits placed inside OTP A are can be erased, write and programmed.
You can't write this bit at 0. You can only write this bit at 1.
If you want to set one or more of these bits at zero, you must erase all off this area with `#TPCMD MASSERASE A` command.

RSETEN

It is the 8th bit in the register. Disable/Enable External Reset:

- 0 → Disable RESETB pin (default)
- 1 → Enable RESETB pin

BSIZE [1:0]

They are the 4th and 3rd bits in the register. Select protected boot area:

- 00 → 2KB – 32B
- 01 → 2KB – 64B
- 10 → 2KB – 128B
- 11 → 2KB – 256B

LOCKB

It is the 2nd bit in the register. Write protection (code) with BSIZE:

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- 0 → Hard LOCK Disable
- 1 → Hard LOCK Enable

LOCKF

It is the 1st bit in the register. Read protection (code):

- 0 → LOCK Disable
- 1 → LOCK Enable

MC94x OTP Standard Commands

#TPCMD MASSERASE A
With this command you can erase the user configuration area placed into OTP A area, so you can set all bits at value 0.

#TPCMD BLANKCHECK A
With this command you can check if the user configuration area placed into OTP A area is blank.

#TPCMD PROGRAM A
You can set one or more bit of user configuration area placed into OTP A area.
If you want to set one bit at zero, you must delete all the OTP A area with Masserase A command.

#TPCMD VERIFY A
Verify if the value set as parameter is equal to the value inside the OTP A user area.

#TPCMD READ A|B|C|D
Read the selected area.

#TPCMD DUMP A|B|C|D
Dump the selected area.

MC94x OTP Program Examples

Set LOCKF at 1: **#TPCMD** PROGRAM A 0x01
In binary is 00000001 and you active only the LOCKF bit.

Set LOCKB at 1: **#TPCMD** PROGRAM A 0x02
In binary is 00000010 and you active only the LOCKB bit.

Set RSETEN at 1: **#TPCMD** PROGRAM A 0x80
In binary is 10000000 and you active only the RSETEN bit.

Set LOCKF and LOCKB at 1: **#TPCMD** PROGRAM A 0x03
In binary is 00000011 and you active the LOCKF and LOCKB bits.

Set all at 1: **#TPCMD** PROGRAM A 0xFF
In binary is 11111111 and you active all bits.

MC94x OTP Correct Sequence for Programming Trimming Area

#TPCMD MASSERASE A
Set all bits at zeros, because it's impossible to set bits at zero with program.

#TPCMD BLANKCHECK A
Check if all bits are zeros.

#TPCMD PROGRAM A <value>
Program Trimming area with inserted value.

#TPCMD VERIFY A <value>
Verify if inserted value is equal to programmed value into Trimming area.

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`#TPCMD ISLOCKED`
(Optional) Print into Real Time Log if device is locked or not into read mode.

`#TPCMD TRIMCHECK`
(Optional) Print into Terminal all significant data from Trimming area.

MC96x Trimming Area

MC96x OTP Overview

ADDRESS	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	...	0x1C	0x1D	0x1E	0x1F
06H	-	-	-	-	-	-	-	-	-	-	-	-	-
04H	-	-	-	-	BGR3	FLASH	LDO1M TEMP	LDO1M LEVEL	-	P1 ID (0xB1)	P2 ID (0xB2)	P3 ID (0xB3)	FT ID (0xF1)
02H	-	OSC TEMP	OSC FREQ	RING OSC	-	-	-	-	-	-	-	-	-
00H	USER COFIG	-	-	-	-	-	-	-	-	-	-	-	-

Configuration : Configuration area address 0x00

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSIZE[1]	BSIZE[0]	-	-	RSTDIS	LockB	-	LockF

MC94x OTP Configuration Area A

The User bits placed inside OTP A are can be erased, write and programmed.
You can't write this bit at 0. You can only write this bit at 1.
If you want to set one or more of these bits at zero, you must erase all off this area with `#TPCMD MASSERASE A` command.

BSIZE [1:0]
They are the 8th and 7th bits in the register. Select protected boot area:

- 00 → 0KB – 2.0KB
- 01 → 0KB – 2.5KB
- 10 → 0KB – 3.0KB
- 11 → 0KB – 3.5KB

RSTDIS
It is the 4th bit in the register. Disable/Enable External Reset:

- 0 → Enable RESETB pin (default)
- 1 → Disable RESETB pin

LOCKB
It is the 3rd bit in the register. Write protection (code) with BSIZE:

- 0 → Hard LOCK Disable
- 1 → Hard LOCK Enable

LOCKF
It is the 1st bit in the register. Read protection (code):

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- 0 → LOCK Disable
- 1 → LOCK Enable

MC94x OTP Standard Commands

#TPCMD MASSERASE A
With this command you can erase the user configuration area placed into OTP A area, so you can set all bits at value 0.

#TPCMD BLANKCHECK A
With this command you can check if the user configuration area placed into OTP A area is blank.

#TPCMD PROGRAM A
You can set one or more bit of user configuration area placed into OTP A area.
If you want to set one bit at zero, you must delete all the OTP A area with Masserase A command.

#TPCMD VERIFY A
Verify if the value set as parameter is equal to the value inside the OTP A user area.

#TPCMD READ A|B|C|D
Read the selected area.

#TPCMD DUMP A|B|C|D
Dump the selected area.

MC94x OTP Program Examples

Set LOCKF at 1: **#TPCMD** PROGRAM A 0x01
In binary is 00000001 and you active only the LOCKF bit.

Set LOCKB at 1: **#TPCMD** PROGRAM A 0x04
In binary is 00000100 and you active only the LOCKB bit.

Set RSTDIS at 1: **#TPCMD** PROGRAM A 0x08
In binary is 00001000 and you active only the RSTDIS bit (dis-active the reset with one).

Set LOCKF and LOCKB at 1: **#TPCMD** PROGRAM A 0x05
In binary is 00000101 and you active the LOCKF and LOCKB bits.

Set all at 1: **#TPCMD** PROGRAM A 0xFF
In binary is 11111111 and you active all bits.

MC94x OTP Correct Sequence for Programming Trimming Area

#TPCMD MASSERASE A
Set all bits at zeros, because it's impossible to set bits at zero with program.

#TPCMD BLANKCHECK A
Check if all bits are zeros.

#TPCMD PROGRAM A <value>
Program Trimming area with inserted value.

#TPCMD VERIFY A <value>
Verify if inserted value is equal to programmed value into Trimming area.

#TPCMD ISLOCKED
(Optional) Print into Real Time Log if device is locked or not into read mode.

#TPCMD TRIMCHECK
(Optional) Print into Terminal all significant data from Trimming area.

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ABOV MC9X Driver Commands

Here you can find the complete list of all available commands for MC9X driver.

```
ABOV MC9x Memory Map

F → Flash
A → Configuration and Trimming Area A
B → Configuration and Trimming Area B
C → Configuration and Trimming Area C
D → Configuration and Trimming Area D
```

#TPCMD CONNECT

#TPCMD CONNECT

This command performs the entry and is the first command to be executed when starting the communication with the device.
Here you can find the log of a standard connect.

```
---#TPCMD CONNECT
Execution of asynchronous pulses.
Requested Clock is 1.00 MHz.
Generated Clock is 1.00 MHz.
Read Id-Code: 0x0132.
Time for Connect: 0.210 s
>|
```

#TPCMD MASSERASE

#TPCMD MASSERASE <F|A>

This command performs a masserase of selected memory.

#TPCMD BLANKCHECK

#TPCMD BLANKCHECK <F|A|B|C|D>

This command performs a verify if all selected memory is erased.

#TPCMD BLANKCHECK <F|A|B|C|D> <start address> <size>

This command performs a verify if selected part of memory based on start address and size is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <F|A>

This command performs a program of all selected memory based on the data in the FRB file.

#TPCMD PROGRAM <F> <start address> <size>

This command performs a program of selected part of selected memory based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

#TPCMD VERIFY <F|A> <R|M|P>

R - Readout verify - If an error is detected, print that error into workbench and return error immediately. (default).
M - Mismatch verify - Print into Terminal, if errors are presents, print all of this errors into workbench and then return error.
P - Print verify - Print into Terminal no errors are displayed.
Verify all memory of the selected type based on the data in the FRB file.

#TPCMD VERIFY <F> <R|M|P> <start address> <size>

R - Readout verify - If an error is detected, print that error into workbench and return error immediately. (default).

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M - Mismatch verify - Print into Terminal, if errors are presents, print all of this errors into workbench and then return error.
P - Print verify - Print into Terminal no errors are displayed.
Verify selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

`#TPCMD READ <F|A|B|C|D>`
This command performs a read of all selected memory.
The result of the read command will be visible into the Terminal.

`#TPCMD READ <F> <start address> <size>`
This command performs a read of selected part of memory based on start address and size.
The result of the read command will be visible into the Terminal.
Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

`#TPCMD DUMP <F|A|B|C|D>`
This command performs a dump of all selected memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

`#TPCMD DUMP <F> <start address> <size>`
This command performs a dump of all selected memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD ISLOCKED

Syntax: `#TPCMD ISLOCKED`

Description: Check if device is locked into readout mode

Examples: Correct command execution: 😊

```
---#TPCMD ISLOCKED
Device is not locked into read mode.
Time for IsLocked: 0.003 s.
```

#TPCMD ISLOCKED

Syntax: `#TPCMD TRIMCHECK`

Description: Print into Terminal all significant data from Trimming and Configuration areas

Examples: Correct command execution: 😊

```
********************** Trimming Area **********************
USER CONFIG:            Address: 0x00          Value: 0x00
 * LockF: 0
 * LockB: 0
 * RSTDIS: 0
 * BSIZE0: 0
 * BSIZE1: 0
OSC TEMP:               Address: 0x21          Value: 0xC0
OSC FREQ:               Address: 0x22          Value: 0x0D
RING OSC:               Address: 0x23          Value: 0x00
BGR3:                   Address: 0x44          Value: 0x57
FLASH:                  Address: 0x45          Value: 0x02
LDO1M TEMP:             Address: 0x46          Value: 0x04
LDO1M LEVEL:            Address: 0x47          Value: 0x54
P1 ID:                  Address: 0x5C          Value: 0xB1
```


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```
P2 ID:                  Address: 0x5D          Value: 0xB2
P3 ID:                  Address: 0x5E          Value: 0xB3
FT ID:                  Address: 0x5F          Value: 0xF1
************************************************************
```

#TPCMD DISCONNECT

#TPCMD DISCONNECT
Disconnect function. Power off and exit.

ABOV MC9X Driver Changelog

Info about driver versions prior to 5.00
All driver versions prior to 5.00 are to be considered obsolete, please update your driver to the latest version.

Info about driver version 1.00 - 09/05/2019
Supported MC94F1102 ABOV based on M8051 instruction set.
When you make a new project for this device, set 2ms for power up time.
Maximum clock frequency is between 1 and 3 Mhz.

Info about driver version 1.01 - 09/05/2019
Fix bug on a recursive stack call into programming entry procedure.

Info about driver version 1.02 - 30/05/2019
Supported MC96F1206 ABOV based on M8051 instruction set.
When you make a new project for this device, set 2ms for power up time.
Maximum clock frequency is between 1 and 3 Mhz.

Info about driver version 1.03 - 27/06/2019
Improved performance and stability.

Info about driver version 1.04 - 04/07/2019
Implemented Program/Read/Erase of OTP A Trimming and Configuration Area.

Info about driver version 1.05 - 19/01/2020
Added new MC9x FPGA.

Info about driver version 2.00 - 07/02/2020
Added new MC9x FPGA static 9 for FlashRunner HS.

Info about driver version 2.01 - 27/11/2020
Upgrade code stability with new FPGA.

Info about driver version 4.00 - 07/04/2021
Added new MC9x FPGA FlashRunner HS GP2 and GP4.

Info about driver version 4.01 - 19/07/2021
Internal update for FPGA name and version tracking.

Info about driver version 4.02 - 12/08/2021
Internal upgrade of the algorithm, no change to the operations it performs.

Info about driver version 4.03 - 16/06/2022
Print current FPGA version loaded into TPSTART command.
Upgraded internal code to align all drivers.

Info about driver version 5.00 - 01/08/2022
Added FPGA for new FlashRunner 2.0 models.

Info about driver version 5.01 - 14/12/2023
Internal driver upgrade.

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